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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
VO, LILIAN	

ART UNIT	PAPER NUMBER
2195	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/484,549	DYKE ET AL.	
	Examiner	Art Unit	
	Lilian Vo	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2 - 12 and 15- 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2 - 12 and 15- 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 2 - 12 and 15- 21 are presented for examination. Claims 1, 13 and 14 have been cancelled.

Double Patenting

2. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

3. Applicant is advised that should claim 15 be found allowable, claim 18 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2 – 12, 15 – 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kisor (US 6,098,091) in view of Bonola (US 5,706,514).

6. As per **claims 15 and 18**, Kisor teaches the invention as claimed, including a method for providing multimedia functionality in a homogeneous multiprocessor environment comprising:

identifying available processing resources in the homogeneous multiprocessor environment independent of the tasks (col. 3 lines 60 - 67);

allocating the available processing resources among the tasks based on the capabilities of each of the available processors of the homogeneous multiprocessor environment and the processing requirements of each of the tasks (col. 6 lines 16- 30);

providing to the available processing resources functional programs and initial data corresponding to the tasks (col. 3 lines 45 – 60, col. 6 lines 31- 35); and

performing the tasks using the available processing resources to produce resulting data (col. 6 lines 16- 30, 43 - 48), wherein the functional programs cause the available processing resources to perform the tasks of at least one of: graphics image processing, video processing, audio processing and communications processing (col. 4 lines 58 - 61).

Kisor did not clearly discloses the step of queuing the tasks. Nevertheless, Bonola discloses the step of queuing the tasks to be processed in a homogeneous environment (col. 3 lines 61 – 65). It would have been obvious to one of an ordinary skill in the art, at the time the invention was made to incorporate the features as disclosed by Kisor together with Bonola to

service and/or handle tasks for reassignment due to system failure as necessary (Kisor: col. 6 lines 48 – 52).

7. As per **claim 2**, as modified Kisor teaches the invention as claimed, including the method of claim 15 wherein a plurality of processors of the homogeneous multiprocessor environment are capable of executing a first instruction of a first instruction set and a second instruction of a second instruction set (Bonola: col. 2 lines 6-10; col. 3 lines 37-44).

8. As per **claim 3**, as modified Kisor teaches the invention as claimed, including the method of claim 2 wherein the first instruction and the second instruction share an identical bit pattern but perform different operations (Bonola: col. 1 lines 15 – 26, col. 2 lines 6 – 10 and col. 3 lines 37 - 44).

9. As per **claim 4**, as modified Kisor teaches the invention as claimed, including the method of claim 3 wherein a first processor of the plurality of processors executes an input/output kernel program, the input/output kernel program including a first portion expressed using the first instruction set and a second portion expressed using the second instruction set (Bonola: col. 3 lines 26-35; col. 7 lines 22-33).

10. As per **claim 5**, as modified Kisor teaches the invention as claimed, including the method of claim 3 further comprising the step of:

converting a functional program of the functional programs expressed using the first instruction set to an equivalent functional program expressed using the second instruction set (Bonola; col. 8 lines 31-45).

11. As per **claim 6**, as modified Kisor teaches the invention as claimed, including the method of claim 3 wherein the tasks comprise x86 processing (Bonola: col. 1 lines 15-26, wherein graphic image processing, video processing, audio processing, and communication processing are just some of the types of tasks that can be performed on an x86 system).

12. As per **claim 7**, as modified Kisor teaches the invention as claimed, including the method of claim 3 further comprising the step of:

receiving the initial data from a first input/output device (Bonola: col. 8 lines 11-15).

13. As per **claim 8**, as modified Kisor teaches the invention as claimed, including the method of claim 3 further comprising the step of:

passing the resulting data to a first input/output device (Bonola: col. 9 lines 13-23).

14. As per **claim 9**, as modified Kisor teaches the invention as claimed, including the method of claim 8 wherein the step of passing the resulting data to the first input/output device further comprises the step of:

passing the resulting data through an intermediary device, wherein the intermediary device is coupled to the first input/output device and to a second input/output device (Bonola: col. 9 lines 13-23).

15. As per **claim 10**, as modified Kisor teaches the invention as claimed, including the method of claim 9 wherein the step of passing the resulting data through an intermediary device, wherein the intermediary device is coupled to the first input/output device and to a second input/output device further comprises the step of:

automatically adapting to a reallocation of the available processing resources among the tasks (Bonola: col. 8 lines 46-65).

16. As per **claim 11**, as modified Kisor teaches the invention as claimed, including the method of claim 8 wherein the step of passing the resulting data to a first input/output device further comprises the step of:

passing the resulting data to a mixed-signal device (Bonola: col. 9 lines 13-15, 19-23).

17. As per **claim 12**, as modified Kisor teaches the invention as claimed, including the method of claim 3 wherein the step of allocating the available processing resources among the tasks is dynamically adjusted (Bonola: col. 8 lines 46-65).

18. As per **claim 16**, as modified Kisor teaches the invention as claimed, including the method of claim 15, further comprising:

keeping track, remotely from the resources, of the capabilities of all available processors of the homogeneous multiprocessor environment (Bonola: col. 7 lines 42-52); and

identifying, independent of the tasks, available processing resources in the homogeneous multiprocessor environment based solely on the capabilities kept track of remotely (Bonola: col. 7 lines 36-38, 42-52).

19. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bonola (US 5,706,514) in view of Kisor (US 6,098,091).

20. As per **claim 17**, Bonola teaches the invention as claimed, including an apparatus comprising:

a plurality of processors coupled to a bus (col. 4 lines 29-33; Fig. 1);

an input/output interface coupled to the bus (col. 4 lines 52-54; Fig. 1);

a plurality of input/output devices coupled to the input/output interface (col. 4 lines 52 - 57, Fig. 1), the plurality of processors processing program code configured to perform a plurality of tasks (col. 9 lines 24-27), the program code comprising:

program code configured to cause a first portion of the plurality of processors to interact with a first input/output device of the plurality of input/output devices (col. 7 lines 22-25);

program code configured to cause a second portion of the plurality of processors to interact with a second input/output device of the plurality of input/output devices (col. 7 lines 42 - 52);

program code configured to cause a second portion of the plurality of processors to emulate a specific microprocessor instruction set (col. 8 lines 11-18);

wherein the first portion of the plurality of processors provides functionality as found in a first application-specific subsystem and wherein the first input/output device is the first application-specific subsystem (col. 3 lines 23-30); and

wherein the second portion of the plurality of processors provides functionality as found in a second application-specific subsystem and wherein the second input/output device is the second application-specific subsystem (col. 7 lines 42-52; col. 8 lines 11-18); and

kernel program code configured to dynamically allocate the processing of the program code among the plurality of processors without regard to a processor mode (col. 3 lines 26-35; col. 7 lines 22-33; col. 8 lines 11 -18).

With respect to the limitation of kernel program code configured to dynamically allocate the processing of the program code among the plurality of processors without regard to a processor mode, Bonola discloses "a technique for handling processor mode mismatched instructions or commands encountered by a CPU within multiprocessor computer system...if a multimode processor encounters a command or instruction that it cannot execute without shifting modes or mode emulation, it will look for an alternate processor present in the computer system to instead handle the mode mismatched command..." In other words, Bonola's system can perform the resource allocation among the processors regardless of a processor mode. Although applicant's specification did not mention the execution is under any type of the processor mode, one of an ordinary skill in the art would recognize that applicant's processors has to be functioned in some type of mode. As noted above, Bonola's system can perform the resource

allocation among the processors regardless of a processor mode. Thus, the limitation narrowed by the claim is considered obvious over Bonola since applicant has not disclosed that limitation solves any stated problem or is for any particular purpose and it appears that Bonola's system is capable of perform the functions as claimed equally well. Therefore, it would have been obvious to one of an ordinary skill in the art, at the time the invention was made to utilize the features as disclosed by Bonola to perform the tasks as desired.

Furthermore, Kisor discloses the limitation of kernel program code configured to dynamically allocate the processing of the program code among the plurality of processors without regard to a processor mode (Kisor: col. 3 lines 45 – 59, col. 6 lines 48 – 59, col. 7 lines 7 – 10, 45 – 50). It would have been obvious to one of an ordinary skill in the art, at the time the invention was made to incorporate Kisor's teaching together with Bonola to dynamically allocate the processing of the tasks as needed (Kisor: col. 7 lines 45 – 50).

21. Claims 19 – 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kisor (US 6,098,091) in view of Bonola (US 5,706,514) as applied to claims 15, 16 and 18 above, and further in view of Sinibaldi et al. (US 6,338,130, hereinafter Sinibaldi).

22. Regarding **claim 19**, as modified Kisor discloses the step of allocating the available processing resources among the tasks based on the capabilities of each of the available processors of the homogeneous multiprocessor environment comprises allocating the available processing resources among the tasks based on the ability of each of the available processors of the homogeneous multiprocessor environment (Bonola: col. 7 lines 36 – 38, 42 – 52, 57 – 61,

col. 8 lines 11 – 18, 46 - 65 col. 9 line 12 – 23). As modified Kisor did not clearly discloses the availability of each available processors to be divided or aggregated with another processor to provide a processing resource. Nevertheless, Sinibaldi disclose the step of allocating the available processing resources among the tasks based on the capabilities of each of the available processors comprises allocating the available processing resources among the tasks based on the ability of each of the available processors to be divided or aggregated with another processor to provide a processing resource (col. 12 lines 59 – col. 13 line 5, lines 28 – 46, col. 19 lines 40 – 52). Therefore, it would have been obvious for one of an ordinary skill in the art, at the time the invention was made to incorporate Sinibaldi's teaching together with as modified Kisor to makes optimal use of the available processing capability of the processors at all time (Sinibaldi: col. 13 lines 45 – 46).

23. **Claims 20 – 21** are rejected on the same ground as stated in claim 19 above.

Response to Arguments

24. Applicant's arguments with respect to claims 15, 16, 17 and 18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lilian Vo whose telephone number is 571-272-3774. The examiner can normally be reached on Thursday 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Lilian Vo
Examiner
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lv
May 10, 2007

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